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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,263	04/21/2004	Sadami Takeoka	60188-821	4838

7590 06/26/2006

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,263	TAKEOKA ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *1-23 and 30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-29* is/are rejected.

7)☒ Claim(s) *24-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/187,269.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a non-Final Office Action in response to the present US Application 10/828,263, filed 04/21/2004, which is a DIV of 10/187,269, filed 07/02/2002, now US PATENT No. 6,734,549.

Election/Restrictions

Applicant's election without traverse of claims 24-29 in the reply filed on 5/11/2006 is acknowledged. Claims 1-23 and 30 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim.

Claims 24-29 are presently under examination. Claims 1-30 are still pending in the Application.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d), JAPAN 2001-201950 07/03/2001. The certified copy has been filed in parent Application No. 10/187,269, filed 07/02/2002, now US PATENT No. 6,734,549.

Specification

The abstract of the disclosure is objected to because it properly fails to describe the claimed invention. The following is an amended abstract suggested by the Examiner:

An apparatus for testing a semiconductor device by mounting a plurality of chip intellectual properties (IPs) on a common semiconductor wiring substrate, including a

silicon wiring substrate on which the chip IPs are mounted. A circuit for a boundary scan test is formed on the silicon wiring substrate by connecting flip-flops to wiring, which are arranged to test connections in the wiring. An IP On Super-Sub (IPOS) device or each chip IP may be arranged to facilitate a scan test, a built-in self-test (BIST), etc., on the internal circuit of the chip IP. Correction is required. See MPEP § 608.01(b).

Claim Objections

Claims 24-29 are objected to because of the following informalities:

Claims 24 and 27-29 recite the acronym IPs, which does not include the full description. The claims should be amended to include intellectual properties (IPs).

Claim 24, on line 5, the expression "bonded thereto;" should be changed to –bonded on the semiconductor wiring substrate;--.

Claim 27 is generally narrative, failing to conform to current U.S. practice. It appears to be a literal translation into English from a foreign document and is replete with grammatical and idiomatic errors. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim26 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 26 recites the limitation "wherein said test controller is provided as a chip IP on said semiconductor wiring substrate", which renders the claim indefinite, because it is unclear whether the limitations following the phrase "as its" are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 24, 25 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Sparks et al. (US 5,321,277) ISSUED: June 14, 1994.

Regarding Claim 24, Sparks discloses a semiconductor device (multi-chip module, 10) Figures 1-3, comprising:

A semiconductor wiring substrate (chip base 13) having a semiconductor substrate (surface) and a wiring layer (interconnect system 12) located at the surface of the chip base 13, where dielectric layers 17a and 17b provide insulation between paths of interconnection system 12, as shown in Figure 1.

A plurality of chip IPs, such as "functional elements" (chips 15) attached to predetermined points of interconnection system 12, where the connections between chips 15 and interconnection system 12 are accomplished by known means, such as wire bonding, tape automated bonding leads, or flip-chip bump interconnection.

A Test controller comprising a Test Access Port (TAP) controller 32, an instruction register 33, a bypass register 34, and a serial data/control bus 31 for connecting scan cells 11 to each other, located on the (chip base 13). The Test Access Port (TAP) controller 32 controls the boundary scan protocol and the sequencing of scan cells 11, associated with each chips 15, in compliance with IEEE 1149.1, test standard. A Test Mode Select (TMS) line into TAP controller 32 controls execution of 1149.1 instructions. A Test Clock (TCK) is a clock input line used to clock test memory logic. A succession of TMS values moves TAP controller 32 through its states.

Regarding Claim 25, Sparks discloses that the controller is made of a semiconductor element embedded within substrate 25, Figure 2A.

Regarding Claim 27, Sparks discloses a scan method including scan cells 11, which are daisy chained to form one or more serial scan paths around the boundary of each chip 15, under test as shown in Figure 3. The test controller supplies a test pattern (Test Data In, TDI) to a chip 15 from a corresponding serial scan path. The test Data Input (TDI) line is used to load serial data into the 1149.1 logic, and the Test Data Output (TDO) line is used to unload serial data from the 1149.1 logic, associated with a chip 15 under test. Sparks further recites in claim 1, connectors embedded within the substrate inter-connecting the test circuits to each other in a configuration that permits

simultaneous pre-testing of all the test circuits in the substrate prior to mounting module chips, and to the input and output connectors in accordance with boundary scan techniques.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sparks et al. (US 5,321,277) ISSUED: June 14, 1994 in view of Rearick (US 6,715,105) FILED: November 14, 2000.

Regarding Claim 26, Sparks does not explicitly disclose "the test controller is provided as a chip IP on the semiconductor wiring substrate".

However, in analogous art, Rearick discloses a test controller (TAP circuit block 20) embedded in chip 10, for testing of logic blocks under test (LBUTs) 74a, b, c, and d, through the corresponding scan paths 72a, b, c and d. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to integrate the test controller of Sparks in the semiconductor chip as taught by Rearick, for the purpose of performing test on logic blocks under test, using TAP controller in compliance with IEEE 1149.1, test standard, which provides scan testing of semiconductor devices,

since according to Rearick, "scan testing is advantageous, because it allows a high degree of controllability and observability of signals inside the chip", see Background of the Invention.

Regarding Claim 28, Sparks substantially discloses a scan method including scan cells 11, which are daisy chained to form one or more serial scan paths around the boundary of each chip 15, under test as shown in Figure 3. The test controller supplies a test pattern (Test Data In, TDI) to a chip 15 from a corresponding serial scan path. The test Data Input (TDI) line is used to load serial data into the 1149.1 logic, and the Test Data Output (TDO) line is used to unload serial data from the 1149.1 logic, associated with a chip 15 under test. Sparks does not explicitly disclose, "a linear feedback shift register (LFSR) function, a multiple input signature register (MISR) function and a BIST function, located in each of the chip IPs".

However, in analogous art, Rearick discloses a chip 10, which includes a test pattern generator 62, output response analyzer 64, and a BIST 60 shown in Figure 1, where the test pattern generator 62 and the output response analyzer 64 correspond to LFSR 102 and MISR 104, as shown in Figure 3. The test controller (TAP circuit block 20) embedded in chip 10, supplies a test pattern (Scan-in port 80 coupled to the TDI port 22) to logic blocks under test (LBUTs) 74a, b, c, and d, through the corresponding scan paths 72a, b, c and d.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a linear feedback shift register (LFSR) and a multiple input signature register (MISR), as taught by Rearick, in each chip of Sparks,

for the purpose of performing test on logic blocks under test, since using a linear feedback shift register (LFSR) and a multiple input signature register (MISR) are well known devices in compliance with IEEE 1149.1, test standard, which provides scan testing of semiconductor devices, since according to Rearick, "scan testing is advantageous, because it allows a high degree of controllability and observability of signals inside the chip", see Background of the Invention.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sparks et al. (US 5,321,277) in view of Chong et al. (US 6,812,718).

Regarding Claim 29, Sparks does not explicitly disclose, " a function for controlling the power supply voltage to each of said chip IPs". However, in analogous art, Chong discloses a system controller 232 (Figure 35), which sends a control signal to power control modules (100a-100n), and selectively switches the corresponding power supplies to one or more devices under test (44a-44n). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate the power control system as taught by of Chong, in the semiconductor wiring substrate of Sparks, for the purpose of selectively connecting the required power supplies to the corresponding chips under test. A person skilled in the art would have been motivated to do so, since testing the chips sequentially results in power savings and unnecessary excessive heat dissipation.

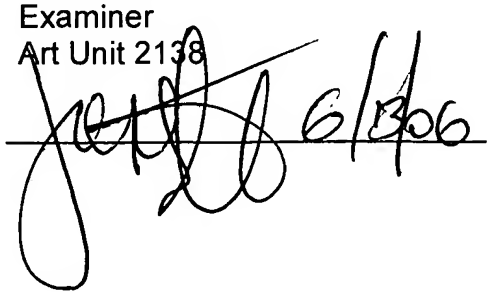
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Examiner
Art Unit 2138



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